REMARKS

Claim 54 has been amended. Claims 1-7 and 51-66 remain in the application. Reconsideration of the application in view of the amendments and the remarks to follow is requested.

Claim 54 has been amended to correct minor informalities noted during review, however, these amendments do not alter the scope of the claims.

Claims 1-7 and 51-66 stand rejected under 35 U.S.C. §102(e) as being anticipated by Forbes, U.S. Patent No. 5,897,351. Claims 52 and 53 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Forbes, U.S. Patent No. 5,897,351. Applicant notes that Forbes '351 issued on April 27, 1999, while the instant application was filed on September 1, 1999.

The §102 rejection of claims 1-7 and 51-66 is believed to be in error. Specifically, the PTO and Federal Circuit provide that §102 anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). The corollary of this rule is that the absence from a cited §102 reference of any claimed element negates the anticipation. Kloster Speedsteel AB, et al. v. Crucible, Inc., et al., 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986). No §103 rejection has been lodged regarding claims 1-7 and 51-66. Accordingly, if Applicants can demonstrate that the Forbes '351 reference does not disclose any one claimed element with respect to claims 1-7 and 51-66, the §102 rejections must be withdrawn, and a subsequent non-final action made with a different rejection in the event that the Examiner still finds such claims to be not allowable.

Applicants note the requirements of MPEP §2131, which states that "TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM." This MPEP section further states that "'A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

The Examiner states that Forbes '351 teaches "forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas, with some widths being no greater than 1 um, at least two being different (Fig. 3 and Col. 7, lines: 55-63)." The Examiner is mistaken on multiple grounds.

First, Fig. 3 shows a single active area ridge having a single width. Thus, Fig. 3 cannot possibly show a plurality of active areas, as recited in Applicant's claims.

Second, the passage appearing at col. 7, lines 55-63 is unrelated to Fig. 3. This passage describes Fig. 4F.

Third, Figs. 4A through 4F unambiguously show that the silicon bars 404 formed on any individual substrate have a single common width, in direct

and stark contrast to the invention as recited in claim 1 ("forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths within the substrate, some of the widths being no greater than about one micron, at least two of the widths being different"), claim 54 ("forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths over the substrate, at least two of the widths being different, at least one of the plurality of active areas having a width less than one micron") or claim 63 ("forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths within the substrate, some of the widths being no greater than about one micron, at least two of the widths being different").

Fourth, Forbes '351 does not teach shallow trench isolation. In fact, Forbes '351 is void of the word "shallow".

Fifth, Forbes '351 teaches use of LOCOS techniques for isolation. See, e.g., col. 7, lines 55-63. Forbes '351 also teaches methods described at col. 6, line 30 through col. 8, line 37 to form silicon bars 404. Forbes also teaches that these may be formed using processes as described at col. 6, lines 47-62. These techniques are not shallow trench isolation.

Sixth, the terms "LOCOS" and "shallow trench isolation" are terms of art having specific and different meanings to those of ordinary skill in the semiconductor arts. Copies of pp. 330-1 and 367-8, taken from S. Wolf,

"Silicon Processing for the VLSI Era", copyright 1995, Lattice Press, Sunset Beach, CA, describing these two different technologies, are enclosed for the Examiner's convenience. Note in particular that the text on p. 367 contrasts these two technologies and further shows why these two technologies are not arbitrarily interchangeable. The definition of the term "shallow trench isolation" provided in Wolf also makes clear that the methods for isolation of silicon islands taught by Forbes '351 are not arbitrarily interchangeable with shallow trench isolation as recited in all of Applicant's independent claims.

Seventh, it is inappropriate to modify the teachings of a reference in attempting to make a valid anticipation rejection under 35 U.S.C. §102. This is explained more fully in MPEP §706.02.

In a subsection entitled "DISTINCTION BETWEEN 35 U.S.C. 102 AND 103", this MPEP section states that: "The distinction between rejections based on 35 U.S.C. 102 and those based on 35 U.S.C. 103 should be kept in mind. Under the former, the claim is anticipated by the reference. No question of obviousness is present."

Eighth, substituting the silicon bar structures 404 taught by Forbes '351 for the shallow trench structures recited in all of Applicant's independent claims gives the term "shallow trench structure" a meaning repugnant to the normal meaning of the term.

Applicant notes the requirements of MPEP §608.01(o), entitled "Basis for Claim Terminology in Description". This MPEP section states that "The meaning of every term used in any of the claims should be apparent from the descriptive portion of the specification with clear disclosure as to its import;

and in mechanical cases, it should be identified in the descriptive portion of the specification by reference to the drawing, designating the part or parts therein to which the term applies. A term used in the claims may be given a special meaning in the description. No term may be given a meaning repugnant to the usual meaning of the term.

Ninth, arbitrarily substituting the processes taught by Forbes '351 for the shallow trench isolation recited in Applicant's independent claims requires modification of the teachings of the reference. It is inappropriate to modify the teachings of a reference in attempting to find anticipation.

Tenth, Forbes '352 fails to show, teach, describe or discuss transistors having different gate widths, as erroneously alleged in the Office Action. In fact, the term "width" is never used by Forbes '351 to describe a transistor gate and is instead only employed to describe the silicon bars 404, the trenches and the total memory cell.

"Gate width" is a term of art used in the semiconductor industry to describe the linear extent of the source and/or drain as these abut the channel. In general, gate width is larger than and is different than the dimension known as "gate length". Gate length refers to the effective separation between the source and the drain of a transistor.

Accordingly, gate width is measured in a direction that is orthogonal to (i.e., at right angles to) the width of the silicon bars 404 formed by Forbes et al. The illustration of Fig. 3 depicts a p-channel transistor and an n-channel transistor that are illustrated as having identical dimensions for both gate width and gate length. The use of merged p- and n-channel transistors by

Forbes '351 is described at least in the Title, Field of the Invention, col. 2, lines 26-33; col. 3, lines 6-16; col. 4, lines 29-32 and 61-65; col. 6, lines 7-9 etc. Forbes '351 is silent with respect to gate width and thus cannot possibly teach or disclose the invention as recited in any of Applicant's claims.

Accordingly, and for at least these reasons, the anticipation and unpatentability rejections of claims 1-7 and 51-66 are clearly in error and should be withdrawn, and claims 1-7 and 51-66 should be allowed.

Dependent claims 2-7, 51-53, 55-62 and 64-66 are allowable as depending from allowable base claims and for their own recited features which are neither shown nor suggested by the prior art.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

In view of the foregoing, allowance of claims 1-7 and 51-66 is requested. The Examiner is requested to phone the undersigned in the event that the next Office Action is one other than a Notice of Allowance. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: June 11, 2001 By: _____

Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

Version with markings to show changes made

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/388,857
Filing Date .....September 1, 1999
Inventor .....Luan C. Tran
Assignee ..... Micron Technology, Inc.
Group Art Unit 2813
Examiner .....L. Schillinger
Attorney's Docket No. MI22-878
Title: Semiconductor Processing Methods Of Forming Transistors, Semiconductor Processing Methods Of Forming Dynamic Random Access Memory Circuitry, And Related Integrated Circuitry

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii) FILING REQUIREMENTS TO ACCOMPANY RESPONSE TO MAY 9, 2001 OFFICE ACTION

Deletions are bracketed, additions are underlined.

In the Claims

54. (Amended) A semiconductor processing method of forming transistors comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths over [a] the substrate, at least two of the widths being different, at least one of the plurality of active areas having a width less than one micron;

forming a gate line over respective active areas to provide individual transistors having different threshold voltages, the transistors being provided with the different threshold voltages without using separate channel implants; and

wherein a transistor with a lower one of the threshold voltages corresponds to the active area having the width less than one micron.

END OF DOCUMENT